REMARKS

Claims 5, 7, 8, 18, 19, and 21 are presently pending in the application. This Amendment currently amends claims 5, 8, 18, 19, and 21. Claims 1-4, 6, 9-17, 20, and 22 are canceled without prejudice or disclaimer. No new matter is added to currently amended claims 5, 8, 18, 19, and 21.

Notwithstanding any claim amendments of the present Amendment or those amendments that may be made later during prosecution, Applicants' intent is to encompass equivalents of all claim elements. Reconsideration in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 5, 7, 8, 18, 19, and 21 stand rejected under 35 U.S.C. §112, first paragraph. Claims 5, 7, 8, 18, 19, and 21 stand rejected under 35 U.S.C. §112, second paragraph. These rejections are respectfully traversed in view of the following discussion.

THE 35 U.S.C. §112, FIRST AND SECOND, PARAGRAPH REJECTIONS

Claims 5, 7, 8, 18, 19, and 21 stand rejected under 35 U.S.C. §112, first paragraph, because the Examiner alleges that the Specification does not clearly disclose a clear meaning of the term "test sweep." Applicants respectfully traverse the rejection of claims 5, 7, 8, 18, 19, and 21 under 35 U.S.C. §112, first paragraph, for the following reasons.

The Specification clearly describes that

"[T]he method of reducing power relies on turning the microcode sequence into a giant state machine in which each opcode is a function of the immediately preceding opcode [that will] maintain the previous control signals to a previous state, and will change only the control signals required for the current cycle's [that is, opcode's] operation. However, the determination of this new state machine is based on an architecture specification with the designer looking at the function, and determining what control signals could be left at the previous state, and what control signals could be changed to new values. Thus, a problem with the first embodiment is that such a determination and changing values of selected ones of the control signals are

performed manually and require human inputs. Once the function is implemented, a large test case falls out." (Specification, page 15, lines 15-28).

In other words and as would be well known to one of ordinary skill in the art, the method of testing a state machine, in which the states of the control signals associated with each particular opcode function to be executed at a current cycle with the states of the control signals associated with each opcode function that may be executed at an immediately preceding cycle, requires an immense number of test cases. Therefore, as explained in the Specification,

"[T]he Auto_Don't_Care method searches the <u>database</u> (e.g., <u>table</u>, etc.), to locate all tests that have this function (e.g., the function of the control signal). and <u>creates a test sweep</u> (e.g, as shown in step 46 described below)." (Specification, page 17, lines 19-21).

In other words and as would be well known to one of ordinary skill in the art, the large amount of testing required to identify those control signals associated with a particular opcode function to be executed at a current cycle with the states of the control signals associated with each opcode function that may be executed at an immediately preceding cycle, would benefit from an automatic method of testing, such as the "Auto_Don't_Care" method, which identifies or marks those control lines associated with a particular opcode function which need not toggle between the current cycle and the immediately preceding cycle. Those preceding opcodes and the associated control signals that may precede the current opcode and its associated control signals may constitute a database. This database may be organized as, for example, a table, with each particular current opcode's control signals forming one axis of the table and each of the particular preceding opcode's control signals forming another axis of the table. Thus, to test each control signal of the current opcode function against the control signals of each particular preceding opcode function, one would step through or sweep through the tablular entries to determine which control signals may be marked "Don't Care." Applicants respectfully submit that this sweeping through may be considered a "test sweep."

Applicants respectfully submit that the above explication of "test sweep" merely represents what one of ordinary skill in the art would deem "test sweep" to mean in the context of the Specification. Applicants also respectfully that the above explication of "test sweep" would be fully enabling to one of ordinary skill in the art. Therefore, for at least the reasons outlined above, Applicants respectfully submit that claims 5, 7, 8, 18, 19, and 21 fully comply with the enablement requirement. Withdrawal of the rejection of claims 5, 7, 8, 18, 19, and 21 under 35 U.S.C. §112. first paragraph, is respectfully solicited.

Claims 5, 7, 8, 18, 19, and 21 stand rejected under 35 U.S.C. §112, second paragraph, because the Examiner alleges that the claims are incomplete for omitting essential structural cooperative relationships of elements, such omissions amounting to a gap between the necessary structural connections. Applicants respectfully traverse the rejection of claims 5, 7, 8, 18, 19, and 21 under 35 U.S.C. §112, second paragraph, for the following reasons.

With respect to claim 5, the Examiner alleges that the relationship between control signals and new data is unclear.

The Specification clearly describes the second embodiment of the invention, i.e., "Auto Don't Care" method of design as,

"[T]he process modifies the design so as to always set in the current cycle all control signals input to their active values. The purpose of such a step is ultimately to set the control bits of an opcode which does not change (e.g., has no affect) to a "don't care" value. Hence, the new template (e.g., the modified design) updates the temporary copy of the updated microcode function block, and then, as shown in step 46, a test sweep is run with the previous state set for the one control signal being examined currently." (Specification, page 17, liens 22-29).

...

Then, all of the templates are executed on the microcodes together with each other. Again the HLLE ensures that the previous control signals are always in the true state (e.g., overrides values). In step S51, a full regression analysis is executed to ensure that the opcode function still functions with the

automatically-generated "don't care" verilog (e.g., with the "don't care" bits set). As mentioned above, the regression is a list (or set) of architectural test cases which are supplied to verify the microprocessor design. (Specification, page 18, line 26 to page 19, line 3)

In other words and as would be well known to one of ordinary skill in the art, the ADC method identifies or marks those control lines which need not be toggled between a previous cycle and a current cycle as a potential "don't care." When the ADC method runs all of its test sweeps, the identity of those "don't care" lines is used to update the hardware description language, so that the amount of logic circuitry associated the ADC method can be minimized. Hence, as would be obvious to one of ordinary skill in the art, the relationship between the control signals and the new data of claim 5, is that of identifying particular control signals as a potential "don't care" state and using this new data to update the hardware description language with an end result of minimizing the architectural logic circuitry for the microprocessor design.

With respect to claim 18, the Examiner alleges that the structural cooperative relationship between function types and microprocessor, between the per-cycle basis updating and the template and the design specification, between the first function boundary and the rest of the claim, and between the opcode group and the rest of the claim is unclear.

As described above, the function types may be considered as relating to opcode functions of the microprocessor. As also described above, the template of is temporary store of the hardware description language, which contains potential "don't care" control signals identified or marked by the ADC method, that is updated at the boundary of each current cycle, or opcode function, with respect to previous cycles, or opcode functions. As further described above, the ADC method examines an opcode function at a current cycle. There exists a boundary between the current cycle and the preceding cycle, i.e., where the state changes occur between, for example, a first opcode function and a second opcode function. In the ADC method of analyzing control signals between a database of current opcode functions and preceding opcode functions, there will exist a first (opcode) function boundary between the first opcode function being examined and possible preceding opcode functions.

With respect to claim 19, the Examiner alleges that the relationship between a template and the per-bit basis, and between the test sweep and the bit-to-bit interconnections, and between function counts and function types, and between full regression and debugging and the templates are unclear.

As described above, the template of is temporary store of the hardware description language. This temporary store included the hardware description of the control signals, i.e., the bit states of the control signals. As also described above, to test each bit of the control signal of the current opcode function against the bits of the control signals of each particular preceding opcode function, one would step through or sweep through the tabular entries to determine which bits of the control signals may be marked "Don't_Care" in a test sweep. Any interaction between individual control bits associated with either the current opcode function or the preceding opcode function may be due to an improper, or inadvertent bit-to-bit interconnection. As also described above, function types may be considered as opcode function types, while a function count, or an opcode function count, is a count of the preceding opcode functions, whose preceding control signals are compared to the current opcode function. That is, the count is a means by which stepping through or sweeping through a tabular database of preceding opcode functions is accomplished. Full-regression is merely a description of fully sweeping through each particular opcode function and its associated control signals to each preceding opcode function and its associated control signals to determine whether a particular control bit line may be considered a "don't care" state in a sequence of templates to debug the hardware logic design.

With respect to claim 21, the Examiner alleges that the relationship between control signals and new data is unclear. Applicants respectfully submit that the relationship between control signals and new data is explained above with respect to the rejection of claim 5.

For at least the reasons outlined above, Applicants respectfully submit that claims 5, 18, 19, and 21 do not omit essential structural cooperative relationships of the invention and instead, particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Withdrawal of the rejection of claims 5, 18, 19, and 21 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

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INFORMAL MATTERS AND CONCLUSION

Applicants respectfully submit that the Specification has been amended, above, to answer the Examiner's objection.

Applicants also respectfully submit that claims 5, 8, 18, 19, and 21 have been amended, above, to answer the Examiner's objections where appropriate.

In view of the foregoing, Applicant submits that claims 5, 7, 8, 18, 19, and 21, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a <u>telephonic or personal interview</u>.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: $\frac{\chi}{100}$

Peter A. Balnave Reg. No. 46,199

McGinn & Gibb, PLLC 8321 Old Courthouse Road Vienna, Virginia 22182-3817 (703) 761-4100 Customer No. 21254